NROM STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 90101240, filed Jan. 19, 2001.

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to an NROM structure. More particularly, the present invention relates to a macro model of an NROM structure in simulating the real operation condition of the NROM.

Description of Related Art

With the development of the technology, the highly cost and largely occupied vacuum tube is replaced by the bi-polar transistor (BJT) with relatively low cost and high operation speed. However, the disadvantage of the BJT is huge energy consumption. Therefore, heat dissipation of the BJT become a main problem when the integration is increased. In order to solve the problem described above, the MOS is developed.

Fig. 1A is schematic, cross-sectional view of a conventional N-type MOS. The N-type MOS comprises a substrate 10, a source 12, a drain 14 and a gate electrode 16. Further, a Vsub, a Vs, a Vd and Vg are respectively applied on the substrate 10, the source 12, the drain 14 and the gate electrode 16. The substrate 10 can be a P-type substrate and the drain 14 and the source 12 can be N-type regions, for example. Also,

gate electrode 16 is constructed by a metal layer or a polysilicon layer 20 and an underlayer, a gate oxide layer 18. In order to describe or apply the MOS on the computer to simulate it's operation condition more easily, the structure of the MOS is simplify into circuit symbols. Fig. 1B is a circuit symbol model of a conventional NMOS.

Figs. 1C and 1D are character diagrams of the NMOS. Since the source and the substrate of the NMOS are usually grounded, performance of the NMOS is controlled by the Vg and the Vd, wherein the Vg decides the switch state of the NMOS and the Vd decides the amount of the current passing through the drain, channel and source when the NMOS is opened. Therefore, as shown in Fig. 1C, the current Id in the NMOS is almost zero when Vg is smaller than Vt. Simultaneously, when Vg is larger than Vt, the current Id in the NMOS is proportionally increased with the Vg. As shown in Fig. 1D, under Vg1, Vg2 and Vg3 (while Vg1<Vg2<Vg3), Id is proportional to Vd when Vd is relatively small. When the Vd is increased to reach a saturated drain voltage, the Id is closing to an saturated situation.

Basing on the factors provided by the character curve in Figs. 1C and 1D, various circuit characters of the NMOS shown in Fig. 1B can be simulated by the computer.

However, with the development of the different NMOS structure, the NROM structure, such as those shown in US Patent 5,966,603 and US Patent 5,768,192, become more complex than ever and the characters of those NROM with complex structure are quite different from the those of the single NMOS shown in Figs. 1C and 1D. Therefore, the model structure basing on the factors of the single NMOS can not

be used to explain the operation phenomenon of the NROM with complex structure. Hence, the NROM with complex structure can not be efficiently simulated by computer.

SUMMARY OF THE INVENTION

The invention provides a macro model of a programmable NROM for simulating the character of the NROM. The NROM comprises a substrate, a drain located in the substrate, a source located in the substrate and a gate electrode located on the substrate between the source and the drain. The gate electrode comprises a first oxide layer, a nitride material layer, a second oxide layer and a polysilicon layer. When the programmable NROM is under a forward reading operation mode, charges are trapped in the nitride material layer close to the drain to form a charge trapped region. The macro model of the NROM comprises a normal MOS symbol element and a short channel MOS symbol element. The normal MOS symbol element represents a first MOS without having the charge trapped region and the first MOS is constructed by a first gate electrode, a first drain and a first source. The short channel MOS symbol element represents a second MOS with the charge trapped region and the second MOS is constructed by a second drain, a second source coupled with the first drain and a second gate electrode coupled with the first gate electrode.

The invention provides a macro model of an NROM for simulating the character of the programmable NROM. The NROM comprises a substrate, a drain located in the substrate, a source located in the substrate and a gate electrode located on the substrate between the source and the drain. The gate electrode comprises a first oxide layer, a nitride material layer, a second oxide layer and a polysilicon layer. When the programmable NROM is under a reverse reading operation mode, charges are trapped in

the nitride material layer close to the source to form a charge trapped region. The macro model of the NROM comprises a normal MOS symbol element and a short channel MOS symbol element. The normal MOS symbol element represents a first MOS without having the charge trapped region and the first MOS is constructed by a first gate electrode, a first drain and a first source. The short channel MOS symbol element represents a second MOS with the charge trapped region and the second MOS is constructed by a second source, a second drain coupled with the first source and a second gate electrode coupled with the first gate electrode.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

Fig. 1A is schematic, cross-sectional view of a conventional N-type MOS;

Fig. 1B is a circuit symbol model of a conventional NMOS;

Figs. 1C and 1D are character diagrams of the NMOS;

Fig. 2 is schematic, cross-sectional view of an NROM for being modeled in a preferred embodiment according to the invention;

Fig. 3 is schematic, a macro model of an NROM in a preferred embodiment according to the invention;

Fig. 4A, a plot of I_D versus V_G, is a character diagram of an NROM under the forward reading operation;

Fig. 4B is a schematic of an NROM under a forward bias operation mode;

Fig. 5A a plot of I_D versus V_G, is a character diagram of an NROM under the reverse reading operation; and

Fig. 5B is a schematic of an NROM under a reverse bias operation mode.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 2 is schematic, cross-sectional view of an NROM for being modeled in a preferred embodiment according to the invention.

As shown in Fig. 2, a part of the NROM which is similar to the conventional MOS comprises a substrate 30, a drain 32 and a source 34. The substrate 30 can be a P-type substrate and the drain 32 and the source can be N-type doped regions formed by implanting N-type ions into the substrate 30. The difference between the NROM and the conventional MOS is a structure of a gate electrode 36 located on a portion of the substrate 30 between the drain 32 and the source 34. The gate electrode 36 is constructed by (from the bottom to the top) a first oxide layer 38, a nitride material layer 40, a second oxide layer 42 and a polysilicon layer 44. When a voltage is applied on the drain 32 to program the NROM, the implanted negative charges are trapped in the nitride material layer 40 to form a charge trapped region 46. The charge trapped region 46 is close to the drain 32 and the charge trapped region 46 only occupy a little part of the nitride material layer 46. Therefore, the channel located at charge trapped region 46 is relatively short. Moreover, because the negative charges are stored near the drain 32 so that the threshold voltage and the barrier around the drain 32 are

relatively high. However, because of its short channel, the drain-induced-barrier-lowering (DIBL) effect is very serious. Therefore, the threshold voltage decreases with the increasing of V_D. Hence, the character curve of the NROM is quite different from that of the conventional NMOS. On the contrary, the character curve of a portion of the nitride material layer 40 without possessing the charge trapped region is similar to that of the conventional NMOS.

Fig. 3 is schematic, a macro model of an NROM in a preferred embodiment according to the invention. As shown in Fig. 3, since the left-hand part of the NROM shown in Fig. 2 is a normal NMOS structure and the right-hand part of the NROM is an NMOS with high threshold voltage and serious DIBL effect because of the existence of charge trapped region, a normal MOS symbol element 50 series with a short channel MOS symbol element 52 is used to represented the NROM described above. It should be noticed that a MOS possesses the channel shorter than the channel of the MOS symbol element 50 is regarded as a short channel MOS. Incidentaly, the normal MOS symbol element 50 comprising a first gate electrode 54, a first drain 56 and a first source 58 represents a MOS constructed by the drain 32, the source 34 and the portion of the gate electrode 36 without the existence of charge trapped region 46. Moreover, the short channel MOS symbol element 52 comprising a second gate electrode 60, a second drain 64 and a second source 62 represents a MOS constructed by the drain 32, the source 34 and the portion of the gate electrode 36 with the charge trapped region 46.

Furthermore, since the normal MOS symbol element 50 and the short channel MOS symbol element 52 share a common gate electrode as the gate electrode 36 shown in Fig. 2, the first gate electrode 54 is coupled with the second gate electrode 60. In

addition, by comparing Fig. 2 to Fig. 3, the first drain 56 is, indeed, the second source 62 so that the first drain 56 is coupled with the second source 62.

Fig. 4A, a plot of I_D versus V_G, is a character diagram of an NROM under the forward reading operation. As shown in Fig. 4A together with Fig. 3, when the NROM is operated under a forward bias (as shown in Fig. 4B, a schematic of an NROM under a forward bias operation mode), a high voltage V_D is applied on the drain 32 and the source 34 is grounded(GND). When the NROM is programmed, charges are stored in the nitride material layer to form the charge trapped region 46. Therefore, the short channel MOS symbol element 52 represents the correlating structure constructed by the drain 32, the source 34 and the portion of the gate electrode with the charge trapped region 46.

Moreover, a high voltage V_D is applied on the second drain 64 and the first source 58 is grounded. If the applied voltage V_D is relatively low (V_D=0.1V), a depletion region 47 formed in drain 32 is relatively small. Besides, because of the effect of the negative charges in the charge trapped region 46, there is no current flows through the channel 49 (as shown in Fig. 4B). As represented by curve 70 in Fig. 4A, the gate voltage V_G is increased over a critical value (as shown in Fig. 4A) to eliminate the negative charge effect of the charge trapped region 46. Therefore, the current flowing through the channel is increased. The current can be well simulated because of the high threshold voltage of the short channel MOS 52. On the contrary, if the applied voltage V_D is relatively high (V_D=2.1V), a depletion region 51 formed in drain 32 is relatively large even larger than the negative charge effect range of the charge trapped region 46. As represented by curve 72 in Fig. 4A, the negative charge effect of charge trapped region 46 can be eliminated under a relatively small V_G (as shown in

Fig. 4A). The current also can be well simulated because of the high DIBL effect of the short channel MOS 52. The threshold voltage decreases when V_D is high. Therefore, the current flowing through the channel is increased.

Fig. 5A a plot of I_D versus V_G, is a character diagram of an NROM under the reverse reading operation. Under the reverse reading operation (as shown in Fig. 5B, a schematic of an NROM under a reverse bias operation mode), charges are stored in the nitride material layer 40 near the source 34 to form a charge trapped region 53 in the left-hand part of the NROM. Hence, left-hand part of the NROM is regarded as an NMOS with a relatively high threshold voltage and serious DIBL effect because of the existence of the charge trapped region near the source 34. On the other hand, since there is no charge trapped in the right-hand part of the NROM, the right-hand part of the NROM is regarded as a normal NMOS. By comparing the top schematic of Fig. 5B to the bottom schematic of Fig. 5B, the short channel MOS symbol element 90 series with the normal MOS symbol element 92 represents the cross-sectional view of the NROM. Because the normal MOS symbol element 92 and the short channel MOS symbol element 90 share a common gate electrode as the gate electrode 36 shown in Fig. 2, the gate electrodes of normal MOS symbol element 92 and the short channel MOS symbol element 90 are coupled with each other. Simultaneously, the drain of short channel MOS symbol element 90 is coupled with the source of the normal MOS symbol element 92.

As shown in Fig. 5A, when the NROM is operated under a reverse bias, charges are stored close to the source 34. The applied voltage V_D at drain will not affect the performance of the short channel MOS symbol element 90 so seriously as under forward reading operation because the negative charges are stored close to the source 34.

Clearly, both normal MOS symbol element 92 and short channel MOS symbol element 90 could affect the performance of the NROM. Therefore, only when a high voltage V_G is applied on the gate electrode even though V_D is high (as represented by curve 82 in Fig. 5A, V_D=2.1V), the normal MOS symbol element 92 and the short channel MOS symbol element 90 are turned on at the same time. Therefore, the I_D is relatively large. If the applied voltage V_D is as low as the applied voltage V_D (V_D=0.1V) used in the forward bias operation mode, a relatively high V_G (as shown by curve 80 in Fig. 5A) is necessary for inducing relatively large current I_D.

Altogether, no matter the operation mode is forward bias or reverse bias, the macro model of the NROM provided by the present invention can explain the operation characters by simple model symbols. Furthermore, based on the macro model, the character factors can be well established and the NROM can be further simulated by computer according to the character factors.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.